LSI DOCKET NO. 01-776

CLAIMS:

What is claimed is:

1. A method for protecting a data transfer, comprising:

receiving a data transfer request, wherein the data transfer request comprises a request address;

determining whether the request address is within a generate address range;

sending generate information to a hardware computation engine;

receiving a cyclical redundancy check value from the hardware computation engine; and

storing the cyclical redundancy check value.

2. The method of claim 1, wherein the generate address range is defined by generate base and limit registers.

3. The method of claim 1, wherein the hardware computation engine calculates the cyclical redundancy check value simultaneously with the data transfer.

4. The method of claim 1, wherein the generate address range maps to a protected data area in memory.

5. The method of claim 4, wherein the data transfer request is a write request.

6. The method of claim 5, further comprising writing data for the data transfer request into the protected data area.

7. The method of claim 1, further comprising:

determining whether the request address is within a check address range if the request address is not within a generate address range;

sending check information to the hardware computation engine;

receiving a cyclical redundancy check result from the hardware computation engine.

8. The method of claim 7, further comprising:

performing the data transfer without cyclical redundancy protection if the request address is not within the generate address range or the check address range.

9. The method of claim 7, wherein the generate address range and the check address range both map to a protected data area in memory.

10. The method of claim 1, wherein the generate information includes the request address and data to be transferred.

11. A method for protecting a data transfer, comprising:

receiving a data transfer request, wherein the data transfer request comprises a request address;

determining whether the request address is within a check address range;

sending check information to a hardware computation engine; and

receiving a cyclical redundancy check result from the hardware computation engine.

12. The method of claim 11, wherein the check address range is defined by check base and limit registers.

13. The method of claim 11, wherein the hardware computation engine checks the cyclical redundancy check value simultaneously with the data transfer.

14. The method of claim 11, wherein the cyclical redundancy check result includes error information.

15. The method of claim 14, further comprising storing the error information.

16. The method of claim 11, wherein the check address range maps to a protected data area in memory.

17. The method of claim 16, wherein the data transfer request is a write request.

18. The method of claim 17, further comprising writing data for the data transfer request into the protected data area.

19. The method of claim 16, wherein the data transfer request is a read request.

20. The method of claim 19, further comprising reading data for the data transfer request from the protected data area.

21. An apparatus for protecting a data transfer, comprising:

a memory interface logic;

a system memory coupled to the memory interface logic;

a hardware computation engine, wherein the hardware computation engine is coupled to the memory interface logic by a memory monitor bus and a memory read/write bus,

wherein the memory interface logic receives a data transfer request, wherein the data transfer request comprises a request address; determines whether the request address is within a generate address range; sends generate information to a hardware computation engine via the memory monitor bus; receives a cyclical redundancy check value from the hardware computation engine via the memory read/write bus; and stores the cyclical redundancy check value in the system memory.

22. The apparatus of claim 21, wherein the generate address range is defined by generate base and limit registers.

23. The apparatus of claim 21, wherein the hardware computation engine calculates the cyclical redundancy check value simultaneously with the data transfer.

24. The apparatus of claim 21, wherein the generate address range maps to a protected data area in the system memory.

25. An apparatus for protecting a data transfer, comprising:

a memory interface logic;

a system memory coupled to the memory interface logic;

a hardware computation engine, wherein the hardware computation engine is coupled to the memory interface logic by a memory monitor bus and a memory read/write bus,

wherein the memory interface logic receives a data transfer request, wherein the data transfer request comprises a request address; determining whether the request address is within a check address range; sends check information to a hardware computation engine via the memory monitor bus; and receives a cyclical redundancy check result from the hardware computation engine via the memory read/write bus.

26. The apparatus of claim 25, wherein the check address range is defined by check base and limit registers.

27. The apparatus of claim 25, wherein the hardware computation engine checks the cyclical redundancy check value simultaneously with the data transfer.

28. The apparatus of claim 25, wherein the cyclical redundancy check result includes error information.

29. The apparatus of claim 28, wherein the memory interface logic stores the error information.

30. The apparatus of claim 25, wherein the check address range maps to a protected data area in the system memory.